CLAIMS

1. In a communications system, a method for non-causal channel equalization, the method comprising:

receiving a non-return to zero (NRZ) data stream input;

establishing thresholds to distinguish a first bit estimate;

tracking the NRZ data stream inputs in response to sequential bit value combinations;

maintaining long-term averages of the tracked NRZ data stream inputs;

adjusting the thresholds in response to the long-term averages; and,

offsetting the threshold adjustments to account for the asymmetric noise distribution.

2. The method of claim 1 further comprising:

comparing the first bit estimate in the NRZ data stream to a second bit value received prior to the first bit, and a third bit received subsequent to the first bit; and,

in response to the comparisons, determining the value of the first bit.

3. The method of claim 2 wherein tracking the NRZ data stream inputs in response to sequential bit value combinations includes:

tracking the NRZ data stream input voltage when the second bit value equals the third bit value; and,

tracking the NRZ data stream mean voltage.

4. The method of claim 3 wherein tracking the NRZ data stream input mean voltage includes an action selected from the group of measuring the NRZ data stream input voltage for all bit sequences and measuring the NRZ data stream input voltage when the second bit value does not equal the third bit value.

5. The method of claim 3 wherein establishing thresholds to distinguish a first bit estimate includes:

establishing a first threshold (V1) to distinguish a high probability "1" first bit estimate;

establishing a second threshold (V0) to distinguish a high probability "0" first bit estimate;

establishing a third threshold (Vopt) to distinguish first bit estimates between the first and second thresholds; and,

the method further comprising:

supplying the first bit estimate for comparison in response to distinguishing the NRZ data stream input at the first, second, and third thresholds.

6. The method of claim 5 wherein establishing a third threshold (Vopt) to distinguish first bit estimates between the first and second thresholds includes:

distinguishing NRZ data stream inputs below first threshold and above the third threshold as a "0" if both the second and third bits are "1" values, as a "1" if only one of the second and third bits is a "1" value, and as "1" if both the second and third bits are a "0" value; and,

distinguishing NRZ data stream inputs above the second threshold and below the third threshold as a "1" if both the second and third bits are a "0" value, as a "0" if only one of the second and third values is a "0" value, and as a "0" if both the second and third bits are a "1" value.

7. The method of claim 6 wherein tracking the NRZ data stream input voltage when the second bit value equals the third bit value includes:

tracking the NRZ data stream input voltage when the second and third bits both have "1" values; and,

tracking the NRZ data stream input voltage the second and third bits have "0" values.

8. The method of claim 7 wherein maintaining long-term averages of the NRZ data stream inputs includes:

creating a first average of the NRZ data stream input voltage when the second and third bits are both "1" values;

creating a second average of the NRZ data stream input voltage when the second and third bits are both "0" values; and,

creating a third average of the NRZ data stream input mean voltage.

9. The method of claim 8 wherein adjusting the thresholds in response to the long-term averages includes:

adjusting the first threshold (V1) in response to the first average;

adjusting the second threshold (V0) in response to the second average; and,

adjusting the third threshold (Vopt) in response to the third average.

10. The method of claim 9 wherein receiving a non-return to zero data stream includes receiving a non-return to zero data stream encoded with forward error correction (FEC);

wherein offsetting the threshold adjustments to account for the asymmetric noise distribution includes:

following the determination of the first bit values, FEC decoding the first bit values; and,

using the FEC corrections of the first bit values to offset the first, second, and third threshold values.

11. The method of claim 10 wherein using the FEC corrections of the first bit values to offset the first, second, and third threshold values includes:

tracking the number of corrections in the first bit when the first bit is determined to be a "1" value;

applying an offset to the third threshold (Vopt) to minimize the number of errors when the first bit is determined to be a "1" value; and,

applying an offset to the first (V1) and second (V0) thresholds that is proportional to the third threshold offset.

12. The method of claim 11 wherein applying an offset to the first (V1) and second (V0) thresholds that is proportional to the third threshold offset includes applying the same offset to the first (V1) and second (V0) thresholds as is applied to the third threshold offset.

13. The method of claim 9 wherein offsetting the threshold adjustments to account for the asymmetric noise distribution includes:

tracking the ratio of first bit “1” values to first bit “0” values;

applying an offset to the third threshold (Vopt) to make the tracked ratio approximately equal to one; and,

applying the same offset to the first (V1) and second (V0) thresholds.

14. A non-causal channel equalization communication system, the system comprising:

a multi-threshold decision circuit having an input to accept a non-return to zero (NRZ) data stream, an input to accept threshold values, and outputs to provide bit estimates responsive to a plurality of voltage threshold levels;

a non-causal circuit having inputs to accept bit estimates from the multi-threshold decision circuit, the non-causal circuit comparing a current bit estimate to bit value decisions made across a plurality of clock cycles, the non-causal circuit having an output to supply a bit value for the current bit estimate determined in response to the non-causal bit value comparisons; and,

a threshold circuit having an input to accept bit values from the non-causal circuit, an input to accept the NRZ data stream, and

outputs to supply threshold values to the multi-threshold circuit that are adjusted in response to asymmetric noise in the NRZ data stream.

15. The system of claim 14 wherein the non-causal circuit includes:

a future decision circuit having inputs connected to the mutli-threshold circuit outputs, the future decision circuit having outputs to supply the current, first bit, estimate and a third bit value;

a present decision circuit having inputs to accept the first bit estimate, the third bit value, and a second bit value, the present decision circuit comparing the first bit estimate to both the second bit value, received prior to the first bit estimate, and the third bit value, received subsequent to the first bit estimate, the present decision circuit having an output to supply the first bit value determined in response to comparing the first bit estimates to the second and third bit values; and,

a past decision circuit having an input to accept the first bit value and an output to supply the second bit value.

16. The system of claim 15 wherein the multi-threshold circuit includes:

a first comparator having an input to accept the NRZ data stream, an input establishing a first threshold (V1), and an output to supply a signal distinguishing when the NRZ data stream input has a high probability of being a "1" bit value;

a second comparator having an input to accept the NRZ data stream, an input establishing a second threshold (V0), and an output to

supply a signal distinguishing when the NRZ data stream input has a high probability of being a "0" bit value; and,

a third comparator having an input to accept the NRZ data stream, an input establishing a third threshold (Vopt), and an output to provide a signal when the NRZ data stream input has an approximately equal probability of being a "0" value as a "1" value.

17. The system of claim 16 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input below the third threshold and above the second threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "1" if both the second and third bit value are "0" values;

a first bit value of "0" if only one of the second and third bit values is a "0" value; and,

a first bit value of "0" if both the second and third bit values are a "1".

18. The system of claim 17 wherein the future decision circuit supplies a first bit estimate for an NRZ data stream input above the third threshold and below the first threshold;

wherein the present decision circuit, in response, supplies:

a first bit value of "0" if both the second and third bit value are "1" values;

a first bit value of "1" if only one of the second and third bit values is a "1" value; and,

a first bit value of "1" if both the second and third bit values are a "0".

19. The system of claim 18 wherein the threshold circuit includes:

a first threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream, the first threshold generator tracking the NRZ data stream input voltage when the second and third bit values both equal "1" and maintaining a long-term average of the tracked NRZ data stream input voltage, the first threshold generator having an output to supply the first threshold (V1) responsive to the long-term average.

20. The system of claim 19 wherein the threshold circuit includes:

a second threshold generator having an input connected to the output of the non-causal circuit and an input to accept the NRZ data stream input, the second threshold generator tracking the NRZ data stream input voltage when the second and third bit values both equal "0" and maintaining a long-term average of the NRZ data stream input voltage, the second threshold generator having an output to supply the second threshold (V0) responsive to the long-term average.

21. The system of claim 20 wherein the threshold circuit includes:

a third threshold generator having an input to accept the NRZ data stream input, the third threshold generator measuring the

mean voltage of the NRZ data stream and supplying the third threshold (Vopt) at an output in response to the measured average.

22. The system of claim 21 wherein the third threshold generator measures the mean voltage by measuring the NRZ data stream input voltage for all bit sequences.

23. The system of claim 21 wherein the third threshold generator has an input to accept the output of the non-causal circuit, and wherein the third threshold generator measures the mean voltage by measuring the NRZ data stream input voltage when the second bit value does not equal the third bit value.

24. The system of claim 21 wherein the multi-threshold circuit accepts an NRZ data stream encoded with forward error correction (FEC); and,

the system further comprising:

a forward error correction (FEC) circuit having an input to receive the first bit value from the non-causal circuit, the FEC circuit decoding the incoming data stream and correcting bit values in response to the decoding, the FEC circuit having an output to supply a stream of corrected data bits; and,

wherein the third threshold generator has an input to accept the stream of corrected bits from the FEC circuit, the third threshold generator offsetting the third threshold (Vopt) in response to comparing the first bit values to corresponding corrected bit values.

25. The system of claim 24 wherein the third threshold generator tracks the number of corrections in the first bit when the first bit is determined to be a "1" value and offsets the third threshold (Vopt) to minimize the number of corrections.

26. The system of claim 25 wherein the third threshold generator has an output to supply offsets proportional to the offset applied to the third threshold;

wherein the first threshold generator has an input to accept the offset from the third threshold generator, and in response supplies an offset first threshold value; and,

wherein the second threshold generator has an input to accept the offset from the third threshold generator, and in response supplies an offset second threshold value.

27. The system of claim 26 wherein the third threshold generator supplies offsets equal to the offset applied to the third threshold.

28. The system of 21 wherein the third threshold generator has an input to accept the output of the non-causal circuit, and wherein the third threshold generator tracks the ratio of first bit "1" values to first bit "0" values and applies an offset to the third threshold (Vopt) to make the tracked ratio approximately equal to one.

29. The system of claim 28 wherein the third threshold generator has an output to supply the offset;

wherein the first threshold generator has an input to accept the offset, and in response supplies an offset first threshold value; and,

wherein the second threshold generator has an input to accept the offset, and in response supplies an offset second threshold value.

30. The system of claim 16 wherein the present decision circuit supplies approximately an equal number of "0" and "1" first bit values in response to establishing the first, second, and third thresholds in the first, second, and third threshold generators, respectively.